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transition systems. Formal Methods in System Design, 1:251-273, 1992. Kluwer Academic Publishers. partially supported by an industrial contract with **Verilog** in a study for the french DGA (Direction automatique de s'equences de test 11 from **Verilog** as an SDL [3] front-end which produces state <ftp.inrialpes.fr/pub/INRIA/projets/NASY/publications/cadp/Fernandez-Jard-Jeron-et-al-96-a.ps.Z>

[Bisimulation Minimization in an Automata-Theoretic.. - Kathi Fisler \(1998\)](#) (Correct) (2 citations)

the required BDDs are prohibitively large for most **designs**. We revisit bisimulation minimization, this time www.cs.rice.edu/~kfisler/Pubs/fmcad98.ps.gz

[The START-VOYAGER Parallel System - Ang \(1998\)](#) (Correct) (1 citation)

a novel protection scheme which improves upon past **designs** by not requiring strictly synchronized Performance predictions based on synthesized **Verilog** code show START-VOYAGER's novel message passing derived from simulation with synthesizable **Verilog** code (Section 5)2. Requirements Our basic csg-ftp.lcs.mit.edu/pub/papers/csgmemo/memo-416.ps.gz

[The Synchronous System Description Language PURR - Kropf, Ruf, Schneider, Wild \(1998\)](#) (Correct)

of Computer Science, Institute for Computer **Design** and Fault Tolerance (Prof. D. Schmid)P.O. Box description languages such as VHDL [10] or **Verilog** [16]Both languages are dedicated to the to hardware description languages like VHDL or **Verilog**, these languages have been **designed** with the goethe.ira.uka.de/~schneider/my_papers/KRSW98a.ps.gz

[SpecSyn: An Environment Supporting the.. - Gajski, Vahid.. \(1998\)](#) (Correct) (2 citations)

Paradigm for Hardware/Software System **Design** Daniel D. Gajski, Frank Vahid, Sanjiv Narayan www.cs.ucr.edu/~vahid/courses/269_f98/specsyn_tvlsi97.ps

[Reversible Computing for Energy Efficient and Trustable.. - Knight, Jr. \(1995\)](#) (Correct)

transactional issues, and programming language **design** which also make fully reversible computer architecture (year 1)ffl MIT will develop full **Verilog** simulations for the reversible architecture, circuits (years 1-2)ffl MIT will develop **Verilog** simulations of a dynamically reconfigurable www.ai.mit.edu/people/cvieri/proposal.ps

[PAM-Blox: High Performance FPGA Design for Adaptive Computing - Mencer, Morf, Flynn \(1998\)](#) (Correct) (13 citations)

PAM-Blox: High Performance FPGA **Design** for Adaptive Computing Oskar Mencer, Martin arith.stanford.edu/oskar/fccm98.ps

[Statechart Methodology for the Design, Validation, and.. - Kol, Ginosar, Samuel \(1996\)](#) (Correct) (1 citation)

Statechart Methodology for the **Design**, Validation, and Synthesis of Large Scale C or Ada) or a hardware description (in VHDL or **Verilog**, at either the behavioral or RTL levels)The compiles the specification into either VHDL or **Verilog**. It can compile into either behavioral or RTL ftp.technion.ac.il/pub/supported/ee/VLSI/async-statecharts.ps.gz

[Robust, High-Speed Network Design for Large-Scale Multiprocessing - DeHon \(1993\)](#) (Correct) (1 citation)

so they can easily be extended or re-parameterized to solve a variety of problems. When building 1445 September, 1993 Robust, High-Speed Network **Design** for Large-Scale Multiprocessing Andr e DeHon on their synthesis tools. Cadence provided us with **Verilog-XL** for simulation. Logic Modeling Corporation www.ai.mit.edu/projects/transit/papers/robust-high-speed-networks.ps.Z

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resources. It cannot, for example, verify a **parameterized design** for all values of the parameter (such as
www-cad.eecs.berkeley.edu/~kenmcmil/papers/1999-01.ps.gz

[Application-Specific Clustered VLIW Datapaths: Early.. - Lapinskii, Jacome, de .. \(2002\) \(Correct\) \(5 citations\)](#)
VLIW Datapaths: Early Exploration on a **Parameterized Design Space** Viktor S. Lapinskii, Margarida F.
very efficiently in this abstract, **parameterized design** space. Moreover, an empirical study
www.ece.utexas.edu/%7Elapinski/publications/cade.pdf

[Fitting Curves and Surfaces with Constrained Implicit Polynomials - Keren, Gotsman \(1999\) \(Correct\) \(4 citations\)](#)
paper suggests a different approach-to **design parameterized** families of polynomials whose zero-sets
www.cs.haifa.ac.il/~dkeren/mypapers/implicit-99.pdf

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: 86 6. Software Tools for **Parameterized Design** 89 6.1 wirec and xs :
gnuplot. 89 6. Software Tools for **Parameterized Design** 6.1 wirec and xs The design entry for ACME
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[Innovative Design as Systematic Search - Dorothy Neville Daniel \(1992\) \(Correct\) \(3 citations\)](#)
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www.cs.washington.edu/homes/weld/papers/sie-aaai93.pdf

[A Beamformer ASIC using Cordic Arithmetic - Xu, Steensma \(1997\) \(Correct\) \(2 citations\)](#)
does support neither multiprocessor nor **parameterized design** and is control oriented. So, A
www.stw.nl/prorisc/cssp97/proc/psz/xu.ps.gz

[Utilizing Rapid Prototyping To Enhance Undergraduate.. - Stamper, Dekker \(2000\) \(Correct\) \(1 citation\)](#)
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fie.engrng.pitt.edu/fie2000/papers/1163.pdf

[Design Space Exploration for The Beamformer System - Smita Bakshi Daniel \(1993\) \(Correct\) \(1 citation\)](#)
In order to do so, we first define a **parameterized design** template for the beamformer and for a FIR
we start by defining and illustrating a **parameterized design** template using several simple examples.
recluse.ics.uci.edu/pub/cad/public_ftp/cadlab-trs/1993/TR-93-34.beamformer_exploration.ps.gz

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these decisions. Within the framework of a **parameterized design** for a RISC instruction processor,
ftp.cs.utexas.edu/pub/techreports/tr93-19.ps.Z

[Exploring the Design Space of LUT-based Transparent.. - Yehia, Clark, Mahlke.. \(2005\) \(Correct\)](#)
not a single design, but rather specifies a **parameterized design** space that offers complex tradeoffs
www.eecs.umich.edu/~ntclark/papers/cases05.pdf

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weight matrix. This capability allows us to **design parameterized** graphs that can encode and detect complex
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DC Hyde - Computer Science Department of Bucknell University, Aug, 1997 - karmak.org

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... in the mid-1 970s through the development of **Verilog** in the ... evaluate and write as- sertions either after the interface/ **parameter** list of a **design** entity or ...Cited by 5 - Web SearchSynthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - group of 9 »

CE Cummings - ... , San Jose, CA, www.sunburst-design. com/papers, March, 2001 - sunburst-design.com

... This time window is specified as a **design** **parameter** precisely to keep a data signal from changing too close to another synchronizing signal that could cause ...Cited by 5 - View as HTML - Web Search

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Our proposed **design** methodology to support the architectural **design** trade-off is to develop a. **parameterized Verilog Framework**. This is shown in figure 2. ...

www.engr.sjsu.edu/electrical/master_proposal_example.pdf - [Similar pages](#)**[PDF] New Verilog-2001 Techniques for Creating Parameterized Models (or ...**File Format: PDF/Adobe Acrobat - [View as HTML](#)

of any parameters until all of the **Verilog** input files have. been read, because the last file read might change every. single **parameter** in the **design**! ...

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change any **parameter** on any module. Translation - when compiling a **Verilog design**, none of the. parameters in any module are fixed until the last **Verilog** ...

www.sunburst-design.com/papers/CummingsHDLCON2001_Verilog2001.pdf - [Similar pages](#)[\[More results from www.sunburst-design.com \]](#)**Creating Verilog HDL Designs for Use with MAX+PLUS II Software**

Instantiate any MAX+PLUS II-supported logic function in your **Verilog HDL design**. You can enter the following functions:. **Parameterized** and non-parameterized ...

www.altera.com/support/software/eda_maxplus2/synplify/vlog/creatv.html - 27k - [Cached](#) - [Similar pages](#)**Verilog HDL: Parameterized Counter**

Altera offers users **design** examples for use in **designs** for Altera devices. ... **Verilog HDL**:

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With respect to coding **parameterized Verilog** models, two **Verilog** constructs that are ...

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Compliant with IEEE 1364 **Verilog** standard • Supports behavioral, RTL and netlist description • Supports **parameterized design** ...

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The main focus of CoMAP is on VHDL and **Verilog** based hardware **design** flows, but its modular **design** enables the integration of any **parameter** related language ...

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WR Stevens... - 1992 - yendor.com

... and raise Functions * alarm and pause Functions * **Signal Sets** * sigprocmask ... AppendixB. Miscellaneous Source Code Our **Header File** * Standard Error Routines. ...[Cited by 392](#) - [Cached](#) - [Web Search](#) - [Library Search](#)[book] Introduction to signal processing - group of 4 »

SJ Orfanidis - 1996 - ece.rutgers.edu

... **Signal averaging** ... generator (interpolation) DFT/FFT Functions bitrev.c - bit reversedindex complex.c - complex arithmetic in C cmplx.h - **header file** for complex ...[Cited by 222](#) - [Cached](#) - [Web Search](#) - [Library Search](#)The MIT-BIH Arrhythmia Database on CD-ROM and software for use with it

GB Moody, RG Mark, C MIT - Computers in Cardiology 1990. Proceedings., 1990 - ieeexplore.ieee.org

... Each **signal** file contains two signals sampled at 360 Hz. 'Header' files include

infor- mation about the leads used, the patient's age, sex, and medi ...

[Cited by 65](#) - [Web Search](#)The Koala component model for consumer electronics software - group of 3 »

R van Ommering, F van der Linden, J Kramer, J ... - Computer, 2000 - ieeexplore.ieee.org

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RW Cox - Comput Biomed Res, 1996 - afni.nimh.nih.gov

... in AFNI are organized into "datasets." A dataset is a 3D brick of 16-bit values,

with some associated information stored in a separate **header file**. ...[Cited by 753](#) - [Web Search](#) - [BL Direct](#)[ps] System Level Design Using the SystemC Modeling Platform

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... 5 shows the corresponding source code **file**. In the top-level routine, all process**header files** and the ... object, which is a special **signal**, is instantiated. ...[Cited by 38](#) - [View as HTML](#) - [Web Search](#)Development of the polysomnographic database on CD-ROM - group of 5 »

Y Ichimaru, GB Moody - Psychiatry and Clinical Neurosciences, 1999 - Blackwell Synergy

... record has a **header file**, which contains general information about the record suchas its length, gains and offset of each physiological **signal**, data structure ...[Cited by 11](#) - [Web Search](#) - [BL Direct](#)A database for evaluation of algorithms for measurement of QT and other waveform intervals in the ECG - group of 3 »

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... Each record includes a **signal file** (record.dat, where record is the record name),a **header file** (record.hea, describing the format of the **signal file**), and sev ...[Cited by 37](#) - [Web Search](#) - [BL Direct](#)A stream input-output system - group of 28 »

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... from input and output queues after a **signal** or on ... into data blocks starting witha **header** giving the ... communicates through the terminal module, a **file** pair, and ...[Cited by 211](#) - [Cached](#) - [Web Search](#)

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... This is different to languages like **Verilog** that only ... 5 shows the corresponding source code **file**. In the top-level routine, all process **header files** and the ...[Cited by 38](#) - [View as HTML](#) - [Web Search](#)

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... via schematic and VHICL Hardware Description Language (VHDL) or **Verilog** hardware description ... The rawbits **file** is converted into a .h **header file** by a program ...[Cited by 4](#) - [View as HTML](#) - [Web Search](#)[BOOK] [The Complete Verilog Book](#)

V Sagdeo - 1998 - books.google.com

... one to define text substitutions and to include **files**, which are defined in ... Synthesis is an essential part of today's design process, and **Verilog HDL** usage for ...[Cited by 7](#) - [Web Search](#) - [Library Search](#)[BOOK] [Principles of Verilog Pli](#)

S Mittra - 1999 - books.google.com

... A PLI ROUTINE 23.1 Step I: Including the **header files** 33.2 Step ... err_intercept 53.3.4 veriusertfs 3.3.5 pli.tab **file** in VCS environment ... FUNDAMENTALS OF VERILOG FL ...[Cited by 8](#) - [Web Search](#) - [Library Search](#)

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A Fin, F Fummi, D Signoretto - ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE ..., 2001 - ieeexplore.ieee.org

... view the core interface (the class declaration in the **header file**) and the ... descriptions to very accurate gate-level representations (VHDL or **Verilog**) by using ...[Cited by 4](#) - [Web Search](#)[Exploiting the Power of Vera: Creating Useful Class Libraries](#)

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... In **Verilog**, global variables are the norm, so **Verilog** programmers may have to learn to resist the ... First, one of the **header file** must be generated manually. ...[Cited by 2](#) - [View as HTML](#) - [Web Search](#)[SystemC Overview - group of 2 »](#)

M Ganguly - Synopsys Inc, 2001 - www-cad.eecs.berkeley.edu

... **Verilog** VHDL Co-sim Interface **Verilog** VHDL Co-sim Interface Import Export Page 30.Testbench // **Header File** #include "systemc.h" SC_MODULE(addr_reg_tb) { ...[Cited by 1](#) - [View as HTML](#) - [Web Search](#)["full_case parallel_case", the Evil Twins of Verilog Synthesis - group of 4 »](#)

CE Cummings - 1999 - sunburst-design.com

... Inferred memory devices in process in routine mux3a line 7 in **file** '.../mux3a.v ... recognize two directives when added to the end of a **Verilog case header**. ...[Cited by 1](#) - [View as HTML](#) - [Web Search](#)[A Verilog to C compiler - group of 3 »](#)

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... The **Verilog** shown in ... include the housekeeping lines generated by the real compiler, which include the inclusion of "ttvinc", other **header files** and so ...[Cited by 2](#) - [Web Search](#)

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Blind Source Separation by Sparse Decomposition in a Signal Dictionary - group of 15 »

M Zibulevsky, BA Pearlmutter - Neural Computation, 2001 - neco.mitpress.org

... We tested two methods with these **data**. ... Let us consider finding the sparsest **signal** that can be obtained by a linear combination of the sensor **signals** $s = w^T X$...Cited by 160 - Web Search - BL DirectA self-describing **data** transfer methodology for ITS applications - group of 8 »

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... to wait for an acknowledgment before Output Axis **Data** can output ... queue, as well as Stop and Resume event **signals** from the ... If so, it waits for a Resume **signal**. ...Cited by 67 - Web Search[book] Data compression: methods and theory

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... the fluctuations and thus meaningful **signals** in the ... among all segmentations of the **data**; then the ... **dictionary** does not distinguish between **signal** and background ...Cited by 123 - Web Search - BL DirectThe PROSITE **dictionary** of sites and patterns in proteins, its current status - group of 7 »

A Bairoch - Nucleic Acids Res, 1993 - pubmedcentral.nih.gov

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CM Westendorf, J Jelitto - Spoken Language, 1996. ICSLP 96. Proceedings., Fourth ..., 1996 - ieeexplore.ieee.org

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... programme is to identify early **signals** of safety ... It complements the previous **signal** generation procedure which in ... new system is based on a **data** mining technique ...Cited by 32 - Web Search - BL Direct

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Computer-aided design of analog and mixed-signal integrated circuits - group of 2 [All articles](#) [Recent articles](#)

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GGE Gielen, RA Rutenbar - Proceedings of the IEEE, 2000 - ieeexplore.ieee.org

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N Kalouptsidis, S Theodoridis - 1993 - Prentice-Hall, Inc. Upper Saddle River, NJ, USA

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1970

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NH Lovell, F Magrabi, BG Celler, K Huynh, H ... - Engineering in Medicine and Biology Magazine, IEEE, 2001 - ieeexplore.ieee.org

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... Development of the system included the **design** and implementation of a hardware interface board and its control software. ... the **design** of the hardware interface. ...View as HTML - Web Search[PS] Integrating Interactive Tools using Concurrent Haskell and Synchronous Events

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The translational termination signal database (TransTerm) now also includes initiation contexts - group of 8 »

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1970

- 2001

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Page 2. 2 Page 3. ELECTRICAL AND COMPUTER ENGINEERING 3 OVERVIEW: ...

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... de Grenoble), UJF (Universite Joseph Fourier, Grenoble-I) and VERILOG SA. ... be formalized
easily: ("The FWC is parametrized with a **signal database** and must be ...

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... Since the two cases of the theorem are captured using the master process and our notion of **signal** dependence, any inter-process ... VHDL Program CFGS Database ...

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... Actual Circuit Ada Model Component type Task type Component instance Task instance

Signal path Message Connectivity Interconnection **database** N input terminals ...

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of your ... user does not need to provide the full path of **HDL signal** a, when ...

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... such a tool is well integrated with all the other applications: • using a common **database**; •

using a ... as Verilog and VHDL have been ... placement in mixed **signal** systems. ...

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VHDL **signal** analysis in VALET - group of 3 »

C Costi, DM Miller - Communications, Computers and **Signal** Processing, 1999 IEEE ..., 1999 - ieeexplore.ieee.org

... be provided within the reusable module **database**. ... description; (iii) input and output

signal width are ... components described in the VHDL hardware description ...

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Using XML for Representation and Visualization of Elaborated VHDL-AMS Models - group of 4 »

T Karayiannis, J Mades, T Schneider, A Windisch, W ... - VHDL International Users Forum Fall Workshop, 2000. ..., 2000 - doi.ieeecomputersociety.org

... Since each class in the **database** is uniquely named ... Hierarchical VHDL-AMS Models for Mixed-**Signal** Simulation ... Proceedings of the International **HDL** Conference and ...

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ATPRG: an automatic test program generator using **HDL-A** for fault diagnosis of analog/mixed-**signal** ...

WH Huang, CL Wey - Instrumentation and Measurement, IEEE Transactions on, 1998 - ieeexplore.ieee.org

... Once the **database** is built successfully, the routine, test ... and CL Wey, "Development of **HDL-A** modeled ... fault diagnosis of analog/mixed-**signal** circuits," IN ...

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Computer-aided design of analog and mixed-**signal** integratedcircuits - group of 2 »

GGE Gielen, RA Rutenbar - Proceedings of the IEEE, 2000 - ieeexplore.ieee.org

... The development of analog and mixed-**signal** hardware description languages like VHDL-AMS [8] and Verilog-A/MS [9] is intended to provide a unifying trend that ...